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Nucleation of Epitaxial Graphene on SiC(0001)

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ABSTRACT A promising route for the synthesis of large-area graphene, suitable for standard device fabrication techniques, is the sublimation of silicon from silicon carbide at elevated temperatures (>1200 °C). Previous reports suggest that graphene nucleates along the ($1\bar{1}0n$) plane, known as terrace step edges, on the silicon carbide surface. However, to date, a fundamental understanding of the nucleation of graphene on silicon carbide is lacking. We provide the first direct evidence that nucleation of epitaxial graphene on silicon carbide occurs along the ($1\bar{1}0n$) plane and show that the nucleated graphene quality improves as the synthesis temperature is increased. Additionally, we find that graphene on the ($1\bar{1}0n$) plane can be significantly thicker than its (0001) counterpart and appears not to have a thickness limit. Finally, we find that graphene along the ($1\bar{1}0n$) plane can contain a high density of structural defects, often the result of the underlying substrate, which will undoubtedly degrade the electronic properties of the material. Addressing the presence of non-uniform graphene that may contain structural defects at terrace step edges will be key to the development of a large-scale graphene technology derived from silicon carbide.

KEYWORDS: graphene · epitaxial graphene · graphene nucleation · silicon carbide

Graphene has received significant interest in recent years as a potential route toward post-CMOS applications that include radio frequency, radiation-hardened electronics, and a multitude of additional niche applications. This has resulted in a flurry of research toward obtaining large-area graphene *via* reduction of graphite oxide,[1,2] chemical vapor deposition on transition metals,[3,4] plasma-assisted deposition,[5,6] and Si sublimation from bulk silicon carbide (SiC) substrates.[7−13] While each route has shown promise, the requirements for complicated layer transfer mechanisms and low carrier mobilities are major hurdles that must be addressed for the non-silicon sublimation methods. However, recent progress in the growth and fabrication of graphene devices on SiC suggests that epitaxial graphene has a place in radio frequency applications.[14]

Growth of epitaxial graphene on SiC (0001) (EG_{Si}), referred to as the silicon face (Si-face) of SiC, is of interest due to the ability to tightly control the layer thickness down to a single monolayer. However, the realization of an atomically flat surface covered by a single layer of graphene requires advances in SiC substrate preparation and intimate knowledge of the graphene nucleation and growth. Substrates are generally grown, cut, and polished such that the the (0001) direction is perpendicular to the surface of the substrate. However, only on rare occasion is the surface oriented exactly in the (0001) direction. Miscut tolerances can be as high as ±0.5° off axis, leaving terraces in the surface that can measure multiple unit cells high. In addition, the process of wafer polishing leaves behind a highly defective surface that requires conditioning prior to graphene growth. Surface treatments can range from no preparation[15] to oxidation and etching of the damaged SiC surface,[16] to deposition of Si onto SiC,[17−19] to hydrogen etching of the SiC surface at elevated temperatures.[7,9,11,13] Most often, the SiC surface is exposed to hydrogen at elevated temperatures (>1500 °C) for 10−30 min, which is quite effective for removing residual polishing damage. Such treatments do change the surface morphology and typically cause significant step bunching.[20−22] In effect, the nominally flat surface with atomically high terrace steps transforms into a three-dimensional surface with terraces exhibiting crystal lattice planes perpendicular to the (0001) and terrace step edges perpendicular to the ($1\bar{1}0n$) crystallographic directions. While the (0001) surface termination exhibits uniform bonding of all silicon surface atoms, those atoms along the ($1\bar{1}0n$) plane exhibit a large number of dangling bonds.[20] The formation of graphene is thought to begin at these "macro" steps in the surface.[12,13,15,18,23] In addition, graphene

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Received for review September 18, 2009 and accepted December 4, 2009.

Published online December 10, 2009.
10.1021/nn901248j

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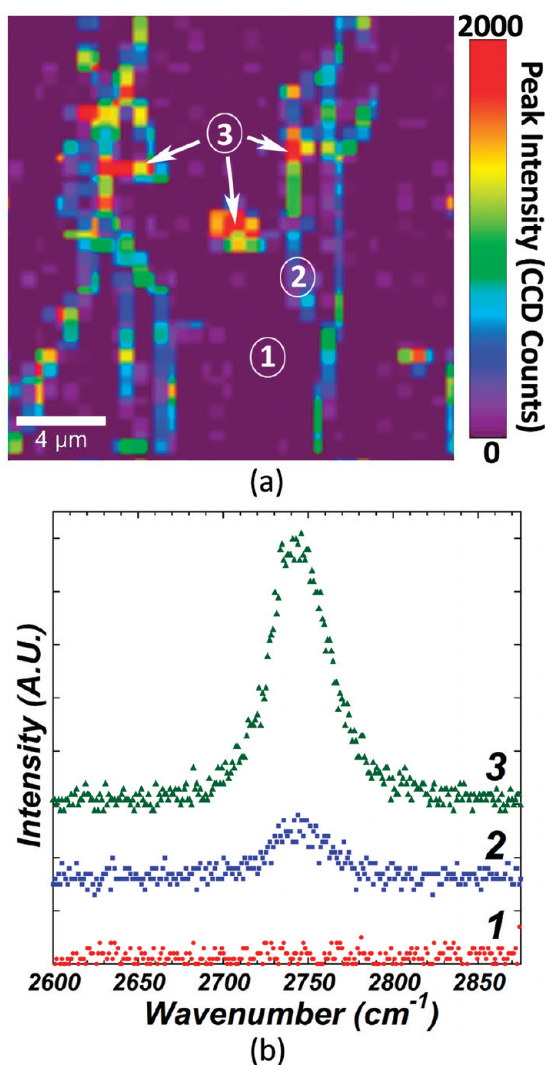

Figure 1. Two-dimensional Raman peak is used to rapidly identify the presence of graphene. Raman topography map of the 2D Raman peak intensity as a function of *x*/*y* position (a) on a graphene sample indicates incomplete coverage. Spectra (b) corresponding to the noted regions in (a) indicate that multilayer graphene is present. Approximately 10% of the surface is covered by graphene.

domain size appears to be correlated with SiC terrace width, indicating that high-quality monolayer graphene is best accomplished using on-axis wafers.[23,24] We have previously shown that this type of surface topography can lead to significant variation in the strain of monolayer graphene and may detrimentally effect the carrier mobility of epitaxial graphene.[24] In this paper, we present data that directly correlate lateral terminations in the SiC (0001) plane (step bunching) with the nucleation of EG_{Si} at temperatures ≤1425 °C and moderate vacuum (1×10^{-6} Torr). In addition, we present the first direct evidence that graphene growth initiates at the SiC step edge, which consists of $(1\bar{1}0n)$ lattice planes.

RESULTS AND DISCUSSION

Samples in this study were prepared using an *in situ* hydrogen (H_2) etch, followed by Si sublimation from the Si-face of semi-insulating 6H-SiC (II−VI, Inc.) at 1225, 1325, and 1425 °C (pressure = 1×10^{-6} Torr). Under these conditions, graphene exclusively forms at terrace step edges and other topological defects. Figure 1a is a two-dimensional Raman map of the 2D peak intensity of a sample graphitized at 1325 °C for 90 min at 0.1 Torr. As indicated by the 2D peak intensity, significant fractions of the 20 × 20 μm scan are void of the characteristic graphene 2D Raman peak, which indicates graphene has not formed in this region. Figure 1b provides representative spectra from the numbered regions in Figure 1a. Peak fitting of spectra 3 in Figure 1b indicates this is multilayer graphene.[25] The presence of a weak peak in the Raman signature (location 2 in Figure 1a,b) likely indicates the initial formation of graphene, where its lateral extent is smaller than the laser spot size in our Raman system.

Graphene nucleation and growth is highly dependent on the SiC surface morphology. Figure 2 shows surface morphology (Figure 2a,c,e) as measured by AFM, as well as the corresponding Raman map (Figure 2b,d,f) for SiC graphitized at 1225, 1325, and 1425 °C, respectively. The AFM images clearly show step bunching (Figure 2a,c,e) with terrace widths averaging >1 μm. In addition, the terrace centers are smooth, showing no evidence of pitting and step heights of 5−15 nm. Importantly, in all cases, graphene is found exclusively at the terrace step edges in the SiC surface. The crystallographic orientation of these terrace edges is found to be perpendicular to the $(1\bar{1}0n)$ direction, which has a reduced atomic bonding coordination.[20] Also evident in Figure 2b,d,f is a variation in surface coverage as a function of growth temperature, with lower coverage at higher temperatures. This observation can be correlated with the terrace step density—samples with higher step density have a higher fraction of the surface covered by the $(1\bar{1}0n)$ planes.[20] We find that the increased step density as a function of growth temperature shown in Figure 2 is coincidence; however, we do find correlation between miscut in the SiC substrate and H_2 etching temperature with step density (see Supporting Information). Figure 2g demonstrates that, as the temperature is reduced, disorder in the graphene increases. The spectra presented in Figure 2g are deconvoluted from the original Raman spectra (see Supporting Information), along with the corresponding D/G peak ratio range found from approximately 200 spectra. The D (1360 cm^{-1}), G (1580 cm^{-1}), and 2D peaks (2700 cm^{-1}) provide information on disorder (D/G ratio), thickness (2D shape and 2D/G ratio), and layer stacking (2D shape).[24,25,28] As the size of the graphene crystallites is reduced, more disorder is present and the D/G ratio increases.[28] We find that D/G ranges from a low of 0.05 (grown at 1425 °C) to as high as 1.0 as the temperature is reduced, indicating that the crystallite size is strongly dependent on growth temperature. To summarize, graphene growth below 1425 °C using typical SiC sublimation conditions leads to the nucleation

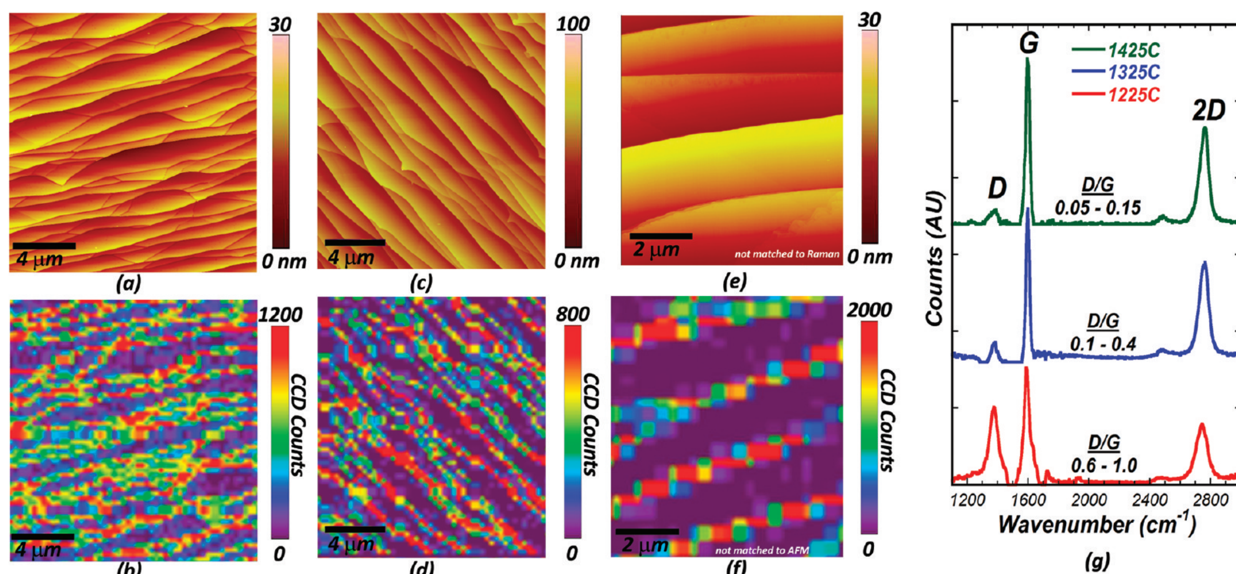

Figure 2. Atomic force microscopy (a,c,d) and Raman spectroscopy (b,d,e) of SiC substrates graphitized at (a,b) 1225 °C, (c,d) 1325 °C, and (e,f) 1425 °C provide evidence that graphene nucleates along step edges parallel to the $(11\bar{2}n)$ plane of SiC. Growth of the graphene occurs in the $(1\bar{1}0n)$ direction. Additionally, Raman indicates that the D/G ratio increases as growth temperature is decreased (g), suggesting that crystallite size is proportional to growth temperature.

of a high density of small crystallites along the step edge and poor quality graphene.

The nucleation and growth of monolayer graphene on the Si-face of SiC is highly dependent on growth conditions, SiC surface morphology, and SiC surface defects. TEM cross-sectional images of SiC graphitized at 1325 °C for 90 min (Figure 3a) confirm that multilayer graphene nucleates at the terrace step edge and subsequently terminates upon reaching the (0001) terrace. In these samples, we also find that up to four graphene layers can form along the step edges before graphene nucleates on the (0001) terrace. This suggests that the reduced bonding coordination of the $(1\bar{1}0n)$ plane may preclude the required surface reconstruction identified for the formation of graphene on the (0001) plane.[26] Furthermore, the existence of SiC surface defects may prevent the formation of continuous graphene layers. Noted in Figure 3a (inset) is the presence of a surface defect on the terrace step that has disrupted the growth of graphene and prevented the formation of continuous graphene layers.

Figure 3b,c illustrates the various morphological defects that influence the nucleation of graphene on SiC, where each terrace step edge is composed of several $(1\bar{1}0n)$/(0001) plane pairs. The abrupt convex bending (Figure 3b) of the $(1\bar{1}0n)$/(0001) plane pair induces a loss of continuity between the upper layers of the graphene film. Additionally, concave bending (Figure 3c) of the $(1\bar{1}0n)$/(0001) plane pairs appears to result in a disordered mix of SiC and graphene. As a result, this type of morphological defect [$(1\bar{1}0n)$/(0001) plane junction; see Supporting Information for schematic description] may limit the crystallite size along the SiC terrace step and is apparently more prevalent at lower graphene synthesis temperatures (Figure 2g). This phenomenon is most evident in Figure 3c, where a minimum of three disruptions in the graphene film can be identified. Last, as evident in Figure 3b, is the propagation of a single monolayer of graphene beyond the terrace step, indicating that graphene growth on SiC(0001) is possible under these conditions.

Transmission electron microscopy of epitaxial graphene indicates growth is "bottom-up".[13,18] Figure 3 and Figure 4 reveal the presence of a uniform, continuous top layer of graphene ex-

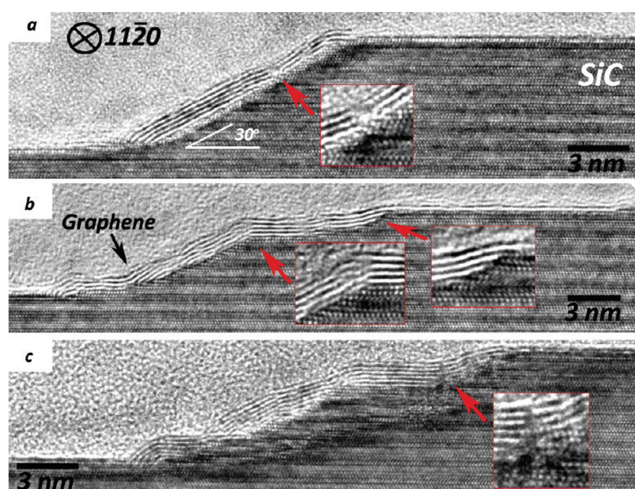

Figure 3. Cross-sectional TEM micrographs of graphene nucleated on the terrace step edge of SiC at 1325 °C. Many-layer graphene is possible along the $(1\bar{1}0n)$ plane even when no growth has occurred on the (0001) plane of SiC. Defects (a) on the SiC surface prevent some graphene from forming continuous layers along the step edge, while $(1\bar{1}0n)$/(0001) plane pairs in the SiC surface (b,c) appear to dictate how the graphene crystallites merge.

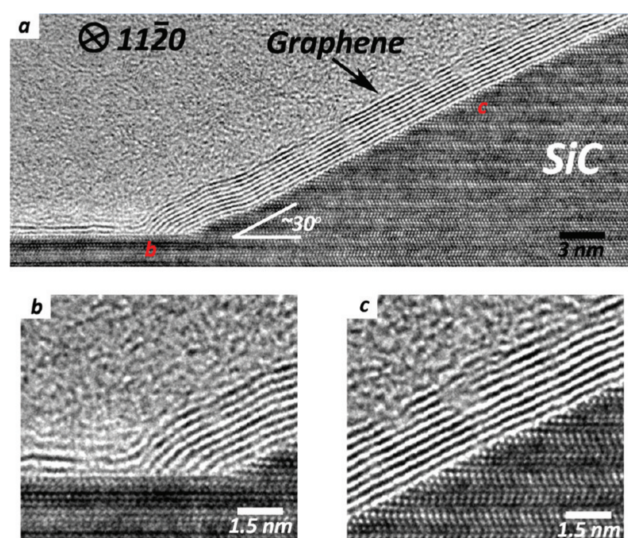

Figure 4. TEM micrographs of graphene on the (1$\bar{1}$0*n*) plane of SiC at 1425 °C. Layer thickness appears not to be self-limiting, evidenced by the many-layer thickness (approximately 8) shown in (a). Additionally, graphene layer termination (b) suggests that the formation of graphene on the terrace step is the result of SiC step erosion. Finally, growth defects (c) may also be present in the graphene films, which provide a means for discontinuous regions within a given layer of the graphene film.

tending over the (1$\bar{1}$0*n*)/(0001) plane junction and onto the (0001) plane. In addition, layers below the top layer (referred to as layer two, three, *etc.*, according to the distance from top layer) terminate into the side of the (0001) plane and appear to form a frontal boundary for graphene growth. This is particularly evident in Figure 3b (inset), which clearly shows that the extent of layer formation is related to the distance from the top layer of graphene. This phenomenon is quite similar to that proposed by others as bottom-up growth, where the first layer of graphene is formed, and each subsequent layer is formed at the graphene/SiC interface.[13,18] Additionally, Figure 4b clearly shows that layers two, three, *etc.*, of graphene terminate into the (0001) plane of SiC, suggesting that the nucleation of graphene results from an erosion of the (1$\bar{1}$0*n*) plane, in agreement with previous reports utilizing ultrahigh vacuum (UHV) Si sublimation.[15] Our work clearly shows that graphene nucleation occurs directly on the (1$\bar{1}$0*n*) plane, not as islands on the (0001) terrace surface as evidenced in UHV growth of graphene.[15] However, it should be noted that the current work utilizes a H_2 etch process, creating steps in the SiC surface prior to graphitization. Occasionally, graphene formation *via* Si subimation is accomplished without the use of surface pretreatment,[15] which as we show in the Supporting Information can lead to non-uniform nucleation and growth of graphene even under the same conditions presented in Figure 2.

Graphene nucleation and growth at macro defects on SiC wafers may not be continuous or self-limiting along the (1$\bar{1}$0*n*) plane. Generally, Si sublimation in a chemical vapor deposition system requires temperatures >1500 °C for complete coverage, and evident from Raman, the D/G ratio is greatly improved at these temperatures. However, transmission electron microscopy provides evidence that (1) growth defects in epitaxial graphene can prevent the formation of uninterrupted layers; (2) growth along the (1$\bar{1}$0*n*) direction may be as thick as 16 layers; and (3) graphene thickness can be highly non-uniform if care is not taken to prevent early nucleation of graphene at terrace step edges. Figure 4 illustrates a cross-sectional TEM micrograph of epitaxial graphene grown at 1425 °C. In general, we find higher growth temperatures produce SiC terrace step edges that are nearly free of (1$\bar{1}$0*n*)/(0001) plane junction, thus providing a means for increased domain growth. Similar to growths at 1325 °C, graphene forms along (1$\bar{1}$0*n*) and subsequently terminates at the (0001) plane (Figure 4a). The increase in growth temperature, however, results in accelerated growth and multilayer formation along the step edges (Figure 4a). These layers terminate at the (1$\bar{1}$0*n*)/(0001) plane junction, and only single and bilayer graphene propagates along the (0001) plane (Figure 4b), suggesting that while graphene formation may be self-limiting on the (0001) surface, many-layer graphene can form on the macro steps in the SiC surface. Additionally, we find evidence that the formation of graphene along the (1$\bar{1}$0*n*) can contain a high density of growth defects (Figure 4c) that could degrade the electronic properties of the graphene film. Finally, TEM results suggest that graphene growth can occur beyond the top and bottom of the terrace step. This is contrary to previous reports suggesting that the nucleation and growth initiates only at the top of the terrace step edge.[13]

The work presented here introduces several key issues that must be taken into consideration during graphene synthesis for high-speed electronics: (1) graphene nucleates along step bunched regions and defects that expose the (1$\bar{1}$0*n*) plane in the SiC surface; (2) graphene nucleation on the (1$\bar{1}$0*n*) plane occurs at much lower temperatures than growth on the (0001) plane; (3) graphene on the (1$\bar{1}$0*n*) plane can have a high density of defects; (4) graphene on the (1$\bar{1}$0*n*) plane does not appear to have a self-limiting thickness; and (5) graphene layers continue to grow and remain confined to the (1$\bar{1}$0*n*) plane until favorable conditions for propagation along the (0001) plane are met. The ability to circumvent the formation of additional layers at the terrace step edge will be important for producing monolayer graphene devices with high mobility and high on/off ratios. While this work indicates that graphene nucleation occurs on the terrace step edge on SiC(0001), it did not focus on optimization of graphene synthesis to reduce the number of layers at the terrace step edge. However, likely solutions to the formation of monolayer graphene along the

(0001) terrace and ($1\bar{1}0n$) terrace step include removing the *in situ* H_2 etch as a means to reduce step bunching in the SiC surface. We find that this particular method results in significant pitting and nonuniform Si sublimation from the SiC surface (see Supporting Information). Alternatively, one may introduce a rapid thermal process to bring the growth temperature to a level where it is thermodynamically favorable for the formation of graphene on (0001) and ($1\bar{1}0n$) simultaneously.[15] Finally, one could alter the growth process to eliminate the intermediate cool down step used in this work, thus keeping the system at a temperature level where growth will occur on both lattice planes.

CONCLUSIONS

We have examined epitaxial graphene on SiC(0001) substrates under conditions that limit its formation to the ($1\bar{1}0n$) plane and have provided evidence that the terrace step edges are a low-energy site for graphene nucleation. Additionally, we have shown that multilayer graphene can form along a terrace step edge prior to the nucleation and growth of graphene on the terrace itself. The presence of many-layer graphene at the terrace step edge will undoubtedly affect the ability to achieve the desired on/off ratios in field effect transistors, as these regions will contain a high density of charge carriers, and thus will introduce a metallic component in graphene transistors.

METHODS

Samples in this study were prepared using an *in situ* hydrogen (H_2) etch, followed by Si sublimation from the Si-face of semi-insulating 6H-SiC (II−VI, Inc.) at 1225, 1325, and 1425 °C (pressure = 1×10^{-6} Torr). To ensure polishing defects are removed from the SiC surface prior to graphitization, samples were heated to 1700 °C in 5% H_2/Ar mixture at 600 Torr, then held at 1700 °C for 30 min for H_2 etching. Under these conditions, terrace dimensions typically range from 1 to 5 μm wide and 7 to 15 nm tall. Following this H_2 etch, samples were cooled to 1000 °C, evacuated to 1×10^{-6} Torr, and subsequently heated to 1225−1425 °C for growth. Postgraphitization characterization was carried out using optical microscopy, atomic force microscopy (AFM), Raman spectroscopy, and transmission electron microscopy (TEM).

A WITec confocal Raman microscope with a 488 nm laser wavelength, diffraction limited lateral resolution of ~340 nm, and spectral resolution of 0.24 cm^{-1} was utilized for Raman spectroscopy. Raman spectra were collected using a spatial step size of 300 nm, laser power of ~60 mW (at sample), with an integration time of 0.5−3 s. We find that maintaining laser expose to <3 s does not degrade graphene structural quality as reported elsewhere.[27] Raman spectra were taken using a low- and high-resolution spectrometer grating. The low-resolution spectral grating consisted of 600 gratings/mm and allowed for data collection of the D, G, and 2D peaks between the wavenumber values of 500−3000 cm^{-1}. The high-resolution grating consisted of 1800 gratings/mm with a spectral window of approximately 1000 cm^{-1}, which provided a means to monitor the 2D peak with increased peak position and shape accuracy. Raman topography maps typically included a 20 × 20 μm region and consisted of 1600−3600 spectra in each map. A minimum of three Raman topography maps and five line scans were taken for each sample.

The ability to measure crystallite size in graphene is essential for growth optimization. Graphene crystallite size was investigated *via* SiC/graphene signal deconvolution and the ratio of the graphene D and G peaks.[28] Deconvolution is accomplished by (1) collection of substrate (SiC) and graphene/SiC (G/SiC) Raman spectra, (2) normalization of the G/SiC spectra to the substrate spectra, and (3) subtraction of the substrate spectra from the G/SiC spectra. Following peak deconvolution, the crystallite size is determined by[28]

$$L_a = \frac{560\ \text{nm}\cdot\text{eV}^4}{E_l^4} \times \left(\frac{I_G}{I_D}\right) \quad (1)$$

where E_l is the laser energy (488 nm laser = 2.54 eV), I_G and I_D are the G and D peak intensity, respectively, and L_a is measured in nanometers.

Acknowledgment. This work was support through The Penn State Electro-Optics Center IRAD 01830.71 and the Air Force Research Lab through ONR Contract # N-00024-02-D-6604 DO 0431. Additionally, support for the WiteC Raman system was provided by the National Nanotechnology Infrastructure Network at Penn State.

Supporting Information Available: Effects of H_2 etch temperature, schematic of a ($1\bar{1}0n$)/(0001) plane pair, graphene/SiC signal deconvolution, and growth of graphene on unetched SiC substrates. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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